Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Currently Amended) A data transfer controller comprising:

an initial value register; and

a control unit,

wherein a transfer source address or a transfer destination address is initially set to said initial value register based upon an external request,

wherein said control unit starts data transferring operations based upon said external request, and controls said data transferring operations from said transfer source address,

wherein said control unit issues an interrupt each time a data transfer corresponding to the external request reaches a predetermined data amount based upon the transfer source address, and

wherein said control unit initializes said transfer destination address after said interrupt has been issued for a predetermined plurality of times, and continues data transferring operations to ~~an~~the initialized transfer

destination address to overwrite the data to the initialized transfer destination address without receiving an additional external request.

2. (Currently Amended) A data processor comprising:

an arithmetic and logic controller;

a data transfer controller,

wherein said arithmetic and logic controller and said data transfer controller are formed on a semiconductor chip,

wherein said arithmetic and logic controller initially sets a first transfer start address of a transfer source address and a second transfer start address of a transfer destination address to said data transfer controller,

wherein said data transfer controller starts data transferring based upon a transfer request from said arithmetic and logic controller, and controls data transferring from said transfer source address to said transfer destination address and changes said transfer destination address in response to data transferring,

wherein said data transfer controller issues an interrupt to said arithmetic and logic controller each time a data

transfer request based upon a given transfer start address reaches a predetermined data amount, and

wherein said data transfer controller changes said transfer destination address to said second transfer start address after said interrupt has been issued a predetermined plurality of times, and restarts said data transferring to a changed transfer destination address to overwrite data to the changed transfer destination address without receiving another transfer request from said arithmetic and logic controller.

3. (Currently Amended) A data processing system comprising an arithmetic and logic controller, a data transfer controller whose transfer control conditions are set by said arithmetic and logic controller, and a peripheral circuit which issues a transfer request to said data transfer controller,

wherein said transfer control conditions includes a transfer source address and a transfer destination address,

wherein said data transfer controller starts data transferring based upon said transfer request from said peripheral circuit, controls data transferring from said transfer source address to said transfer destination address

and changes said transfer destination address in response to data transferring,

wherein said data transfer controller issues an interrupt to the arithmetic and logic unit each time a data transfer request based upon a given transfer start address reaches a predetermined data amount,

wherein said data transfer controller initializes said transfer destination address after said interrupt has been issued a predetermined plurality of times, and continues said data transferring to said initialized transfer destination address to overwrite data to the initialized transfer destination address without any additional request from said peripheral circuit or said arithmetic and logic controller.

4. (Currently Amended) A data transfer controller comprising:

an initial address register capable of being externally set with an initial transfer control address information as a first transfer control address information;

an address generating unit which renews the first transfer control address information each time data is transferred from a transfer source to a transfer destination;

a temporary address register is set to the first transfer control address information as a second transfer control address information, and this second transfer control address information is renewed therein by said address generating unit;

a transfer number counting unit capable of repetitively performing an operation of counting the number of transfer times up to a first target number each time data is transferred from the transfer source to the transfer destination;

a repetition number counting unit capable of repetitively performing an operation of counting the number of repetition times of the operation of said transfer number counting unit which counts the number of transfer times up to the first target number, up to a second target number; and

a control unit which starts a data transfer operation from the transfer source to the transfer destination in response to a data transfer request, outputs an interrupt signal each time said transfer number counting unit counts up to the first target number, and sets the first transfer control address information to said temporary register from said initial address register each time said repetition number

counting unit counts up to the second target number, for overwriting data to a transfer destination in accordance with the second transfer control address information.

5. (Previously Presented) A data transfer controller according to claim 4,

wherein said temporary address register is a destination address register for storing a transfer destination address,

wherein said initial value register is an initial address register to which a start address of the transfer destination is set, and

wherein said control unit is capable of starting a data transfer control of storing data at a transfer source address to the transfer destination at a transfer destination address in the destination address register, in response to the data transfer request.

6. (Previously Presented) A data transfer controller according to claim 4,

wherein said temporary address register is a source address register for storing a transfer source address,

wherein said initial value register is an initial address register to which a start address of the transfer source is set, and

wherein said control unit is capable of starting a data transfer control of storing data at the transfer source address in the source address register to the transfer destination at a transfer destination address, in response to the data transfer request.

7. (Previously Presented) A data transfer controller according to claim 4, further comprising a source address register for storing a transfer source address and a destination register for storing a transfer destination address,

wherein said control unit can select either said source address register or said destination address register as said temporary address register and can start a data transfer control by using said temporary register, in response to the data transfer request.

8. (Currently Amended) A data transfer controller according to claim 4, further comprising a transfer number ~~designation~~

register capable of being externally set with the first target number.

9. (Previously Presented) A data transfer controller according to claim 4, wherein the second target number is three.

10. (Previously Presented) A data transfer controller according to claim 1, further comprising a RAM usable as the transfer source or the transfer destination.

11. (Previously Presented) A data transfer controller, according to claim 4, further comprising a selecting circuit,

wherein, said initial address register is capable of storing a plurality of said transfer control address information,

wherein said selecting circuit is capable of selecting an arbitrary one of said transfer control address information stored in said initial value register as said first transfer control address information.

12. (Previously Presented) A data processor comprising an arithmetic and logic controller and a data transfer controller according to claim 11,

wherein said arithmetic and logic controller is capable of set a transfer conditions to said initial address register in said data transfer controller as said plurality of initial transfer control address information, and is capable of outputting said data transfer request to said data transfer controller.

13. (Previously Presented) A data processor according to claim 12, further comprising a RAM accessible by said arithmetic and logic controller and said data transfer controller,

wherein said arithmetic and logic controller, said data transfer controller and said RAM are formed in a single semiconductor chip.

14. (Previously Presented) A data processor according to claim 13, further comprising a peripheral input/output circuit accessible by said arithmetic and logic controller and said data transfer controller,

wherein said peripheral input/output circuit is capable of outputting the data transfer request to said data transfer controller.

15. (Previously Presented) A data processing system comprising:

a data processor recited in claim 14; and

a voice signal input circuit connected to said peripheral input/output circuit of the data processor, wherein the data processor stores an operation program for said arithmetic and logic controller,

wherein in accordance with the operation program, said arithmetic and logic controller sets transfer conditions to said data transfer controller, the transfer conditions being used when a voice signal input from said voice signal input circuit to said peripheral input/output circuit is transferred to said RAM,

wherein said data transfer controller controls to transfer the voice signal to said RAM in response to the data transfer request from said peripheral input/output circuit, and

wherein when an interrupt signal is received from said data transfer controller, said arithmetic and logic controller reads the voice signal from said RAM and processes the read voice signal.